



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Tong Xiao, Robert E. Mains
Assignee: Sun Microsystems, Inc.
Title: Abstraction Generation for Hierarchical Timing Analysis Using Implicity
Connectivity Graph Derived from Domain Propagation
Serial No.: 10/694,139 Filed: October 27, 2003
Examiner: Unknown Group Art Unit: 2183
Docket No.: SUN030009 Customer No. 33438

Austin, Texas
February 27, 2004

COMMISSIONER FOR PATENTS
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Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:


Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants wish to call the following documents to the attention of the Examiner.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

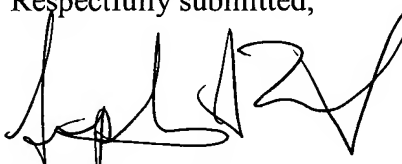
1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, PO Box 1450, Alexandria, VA 22313-1450, on February 27, 2004.

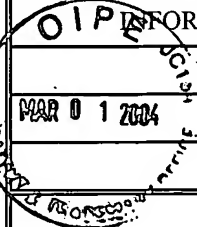

Attorney for Applicant(s)

2/27/04
Date of Signature

Respectfully submitted,



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U.S. Department of Commerce, Patent and Trademark Office				Attorney Docket No.		Serial No.		
				SUN030009		10/694,139		
				Applicant(s)				
(Use several sheets if necessary)				Tong Xiao et al.				
				Filing Date		Group		
				October 27, 2003		2183		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL						<input type="checkbox"/>	<input type="checkbox"/>
	A						<input type="checkbox"/>	<input type="checkbox"/>
	AN						<input type="checkbox"/>	<input type="checkbox"/>
	AO							
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AR	Moon, Cho W.; Kriplani, Harish; Belkhale, Krishna P. "Timing Model Extraction of Hierarchical Blocks by Graph Reduction" IEEE/ACM Proceedings of the 2002 Design Automation Conference, June 2002						
	AS	Yalcin, Hakan; Mortazavi, Mohammad; Bamji, Cyrus; Sakallah, Karem A. "Fast and Accurate Timing Characterization Using Functional Information" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 20, Number 2, February 2001						
	AT							
Examiner			Date Considered					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								